Publishable Summary

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Project acronym:	**DRAGON**
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1 Publishable summary

1.1 Project context and objectives

Project Name: **DRAGON** *Start Date*: February 1, 2010
Grant Agreement: **248277** *Duration:* 40 months
Project Website: http://www.dragon-project.eu
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Mission of DRAGON

"The main idea of the DRAGON project is to research and use new design methodologies and architectural innovations, based on reconfigurability and state-of-the-art digital CMOS technology, in order to break the barriers imposed by the lack of scaling properties of analog components. With this concept, distinct reductions in cost, size and energy consumption for multi-standard cellular handsets can be achieved, while higher demands on data rate can be met. Data rates are increasing every day, therefore, the energy consumption per transmitted or received data bit has to be reduced in order to save energy and avoid thermal problems. Wireless data services will become an attractive low-cost alternative to be used in novel applications."

The goal of the DRAGON project was the development of a design platform comprising multi-standard transceiver specifications and novel flexible architectures. A number of required external components, like analog filters were replaced by reconfigurable digital (CMOS Complementary Metal Oxide Semiconductor) circuitry; and critical building-blocks were implemented to demonstrate proof of concept, both of the architecture and design methodology. All critical building-blocks were fabricated, tested and demonstrated in state-of-the-art CMOS technology.

The DRAGON project pursued the following objectives:

- Miniaturisation of Complex Radio Systems
- Design Methodologies for Energy Efficient Solutions for High Performance Systems
- Multi-Functional / Multi-Purpose Devices
- Proof of Concept by Silicon Demonstrators

1.2 Description of the work performed and main results achieved

The DRAGON project started in February 2010 and has run for 40 months, ending in May 2013.

The progress achieved by all work packages within the 40 months project duration can be summarized as follows:

WP1 Requirements and standardisation a set of system specifications, based on LTE rel10, both for RX and TX intending to serve as over-all requirements, providing targets that aim to justify the project output both for academia as well as industry. After a first system analysis, and specification update, for both RX and TX in period 2 of the project, the main objective for the third period within WP1 was to perform system analysis based on achieved building block performance by the research groups. By maintaining a continuous discussion among the partners, the progress has been monitored and kept towards committed goals. As a result the project has looked into several interesting implementation concepts, all targeting the LTE-rel10 standard and outlined band support. WP1 has then in cooperation with the implementation WPs evaluated the concepts according to needed performance from an industry perspective and completed two system evaluations. In parallel, WP1 has had a continuous dialog with the internal EAB LTE standardization delegacy to secure the relevance of the target specification.

WP2 Low power concept and architecture investigated and defined the receiver architecture and the transmitter architecture. According to the feedback from the circuit designs and more detailed simulation results the architectures were refined. During the third project period, the main task of WP2 was to investigate and develop system concepts, algorithms, and architectures for receivers and transmitters aiming at the LTE-rel10-based standard and best possible analog downscaling in terms of

power consumption, size and area. Thus, milestones M02.3 “Receiver architecture optimised” and M02.4 “Transmitter architecture optimised” were reached successfully. In close cooperation with the partners and WP1, WP3 and WP4 different concepts for key building blocks were investigated and evaluated. While WP2 provided the concepts for the circuit implementations for WP3 and WP4, it also developed the fundamental mathematical principles of the investigated concepts.

WP3 Innovative miniaturised receiver design focused on the designs of the selective RX ADC and the bandpass ΔΣ ADC, resulting in the first round of respective test circuits. Subsequently, new versions of the receiver prototypes were designed and processed: several key building blocks were realized in the third project period, all contributing to the final goal of enabling the design of a full RX system, implemented in a standard digital nanoscale CMOS technology for low cost and with low power consumption. The research on a selective RX ADC has resulted in the development of a new oversampling ADC architecture, with the channel-select filtering functionality included in the feedback loop. The performance is such that it can be the only block in the baseband chain of an LTE receiver, no other components are needed anymore. Research towards a direct digitisation receiver based on a bandpass ΔΣ ADC has shown that it was not possible to remove the RF front-end filters of the receiver without loss in LTE performance. Instead, the need for analog circuit content of the RX chain has been relaxed by increasing the resolution of the baseband ADC, using 40nm technology. A very low power and area is obtained with the extension of a SAR ADC with a 2nd stage that further quantises the residue voltage based on the stochastic behaviour of multiple independent digital comparators. A 9dB increase in SNDR (or 1.5 extra bits) is achieved at almost no extra cost. Finally, the power/noise trade-off of the commonly used class-B VCO has been improved in several new VCO implementations. The oscillation swing of a class-C VCO has been improved, and a novel class-D VCO has been developed, all achieving state-of-the-art figures-of-merit.

WP4 Smart transmitters and power amplifiers designed two PAs in line with the design concepts of DRAGON, one targeting for high output power, the other as a Doherty PA especially targeting for high efficiency at power back-off in the beginning of the project. Both designs were first taped out in UMC 90nm-technology and measured and provided the basis for the development of multi-level burst-mode architecture. Besides, the major bottlenecks for the generation of multi-level burst-mode signals were identified and a discrete lab demonstrator was built. During the second project year, deliverable D4.2 “Power amplifier topology: version 1 description and design” and milestones M04.1 “Power amplifier tape-out 1” and M04.3 “Digital modulator and driver tape out 2” have been met. According to the measurement results achieved, the burst-mode architectures, PA architectures and digital modulator architectures were improved leading to a higher degree of integration. In the third project period, based on the experience from the first PAs, a final PA achieving both high output power and high efficiency at power back-off was realized and simultaneously in WP4, the task was to investigate and evaluate several circuit techniques for the burst mode transmitter design. As a result, in close cooperation with WP2, the partners in WP4 have looked into several interesting possible concepts and circuit architectures for both the modulator and the power amplifier, all targeting the stringent LTE-rel10-based requirements defined as the standard to be met at the start of the project. By maintaining a continuous discussion among the partners involved in WP4, the progress has been monitored and kept towards the committed goals.

WP5 Proof of concept and verification established a feasible policy for silicon access for all implementing partners as well as access to Infineon PDK was established. Furthermore, first prototype PAs were implemented to identify the different research lines for the proof-of-concept demonstrators, the first prototype receiver front-end was taped out and the technology for the tape-out of the first test chips was defined so that the first tape-out was reached successfully in the second project year. All planned test chips for the first half of the project were implemented and successfully characterized. Feedback from the first prototype test chips was considered in the 2nd series of prototype test chips for the addressed TX- as well as for the RX block. Access for 40nm CMOS technology could be provided to additional partners via Europractice enabling the project also to implement TX-blocks in 40nm CMOS technology. During the last project reporting period (M25-M40) several chips for RX and TX building blocks were taped out mainly in 40nm CMOS, such as a high performance RX ADC, two filtering ADCs, two low power VCOs (class-C and a class-D) and a dual-mode Doherty PA. Prototype chips were characterized and the results documented and feedback was provided to WP1 for the overall system evaluation.

WP6 Project Management and Dissemination was responsible for the effective organisation of the project and covered the relevant management components. Another part of this WP was the

dissemination of the project achievement and results, implying the creation of a project website, a leaflet, a logo and dissemination plan as well as an internal communication infrastructure.

1.3 Final results

The results of DRAGON were achieved in multiple steps and marked by three major milestones, which constituted central points in the course of the project and spanned across the technical work packages (please see Figure 1 below).

Milestone 1 – Architectural Exploration

Architectural innovative ideas were identified, explored and used as a high level tool to realise project targets. The focus of the corresponding design experiments was defined.

Milestone 2 – CMOS Building Block Design and Implementation

The most critical building blocks for the targeted multi-standard radio systems with novel architectures were implemented and measured, using state-of-the-art digital CMOS technology.

Milestone 3 – System Demonstration

Silicon system demonstrators were realised and measured. The overall project results were consolidated and verified against the initial goals.

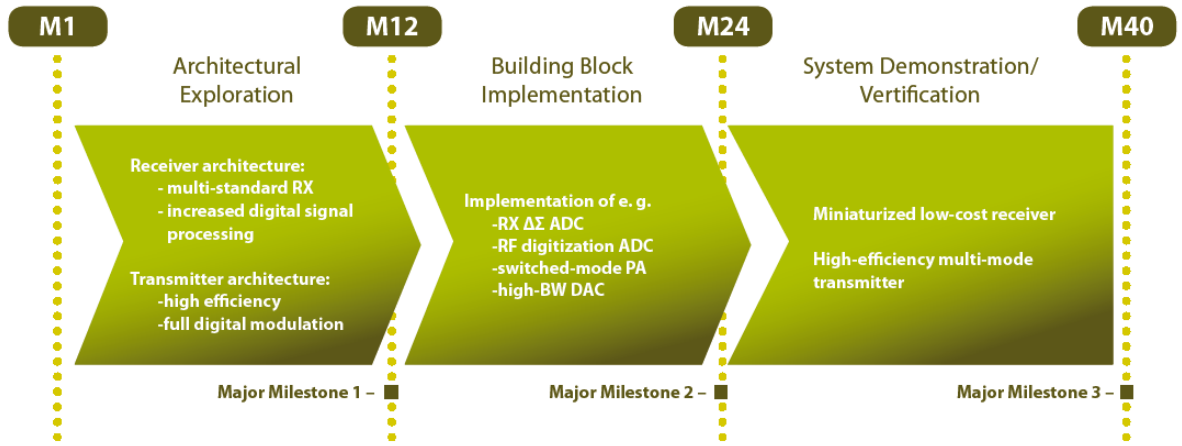

Figure 1: DRAGON Project stages

The overall strategy of the project was to define a common system specification and use this in the initial architecture exploration and building block design, as outlined in Major Milestones 1 and 2. The defined specification was based on the state-of-the-art 3GPP LTE release 10 standard. By using this standard as a basis it was assured that results are relevant for the project industry partners. Then the requirements as well as constraints and features from state-of-the-art CMOS technology were applied to arrive at a forward-looking architecture as well as circuit level requirements for the critical building blocks. After the first round of circuit fabrication the measured block performances were fed into a system level simulation and verified against the specification as well as the individual block targets. Finally, the system demonstration was performed. Silicon system demonstrators were realised and measured and the overall project results were consolidated and contrasted with the initial goals:

- Miniaturized low-cost receiver

The receiver circuits developed in the DRAGON project have led to a significant area and power reduction by cleverly exploiting the digital CMOS process technology speed and density advances for the implementation of blocks with analog and RF functionality. For example, the filtering ADC obsoletes a separate channel-select filter and achieves a 40% reduction in power consumption and 20% reduction in chip area compared to a corresponding conventional solution, and in the baseband ADC the resolution is increased by 9dB at negligible area cost by estimating the residue voltage using digital comparators.

- High efficiency multi-mode transmitter

The transmitter circuits developed in the DRAGON project have exploited digital modulation techniques and state-of-the-art digital CMOS technology to achieve a significant improvement in the power-added efficiency for an integrated CMOS-based transmitter. The 40nm CMOS dual mode Doherty PA achieves almost 26dBm of peak output power while also being capable of delivering 22.5dBm LTE-compliant average output power at 18.9% PAE, which is more than 2.5 times better than a similar class-B PA.

1.4 Impact and use

Society today increasingly asks for wireless systems since they have the potential to enhance comfort and pleasure. More importantly even, wireless technologies can help to support independent living and save costs in health care for an ageing society.

Industrial progress relies on continued growth of wireless capacity. Not only more and more people count on mobile broadband services in their professional activities, also the number of objects connected by wireless interfaces is dramatically increasing.

DRAGON provides an essential contribution to meet these growing societal demands:

The DRAGON project team has studied energy and cost efficient solutions for future radio terminals. To make sure the results are relevant to industry, the partners have used requirements based on LTE release 10, supporting up to 40MHz RF bandwidth, and worked with state-of-the-art CMOS technology.

The research has focused on the development of new solutions for key radio building blocks, like receiver data converters and filtering, local oscillators for frequency synthesis, and high-efficiency power amplifiers and modulators. Test chips have been built and evaluated to demonstrate the feasibility of these building blocks.

In order to assess the performance of the building blocks when parts in a complete radio modem, the project team has defined three different use case scenarios. These scenarios together with actual measured building-block parameters have been used in a system-level simulation tool, also developed in the DRAGON project. By comparing the simulated system performance with the LTE based specification it can be verified that the novel DRAGON test circuits would work, also in a real radio modem.

Some results achieved are already state-of-the-art and published at the most prestigious IEEE conferences and journals. The designs and design reports will be useful for the industry partners when designing future cellular, and other wireless, transceivers, and the fact that the designs are verified to the system specifications will simplify adoption by industry.

1.5 DRAGON Project Consortium and Website

The challenging goal of the DRAGON project has been achieved thanks to the cooperation within a strong consortium that has brought together partners and competencies from Europe's leading companies in the areas of nano electronics and wireless communications, one research institute and three universities, with radio chip designers and system experts. The DRAGON consortium consisted of the following organisations: Technikon Forschungs- und Planungsgesellschaft mbH (TEC), Austria, Ericsson AB (EAB), Sweden, Infineon Technologies Austria AG (IFAT), Austria, Lund Universitet (LU), Sweden, Katholieke Universiteit Leuven (KUL), Belgium, Interuniversitair Micro-Electronica Centrum VZW (IMEC), Belgium, Technische Universität Graz (TUGraz), Austria. Thus, the consortium has covered the full design chain from customer requirements over system integration to hardware design. Top universities were included to secure innovation and move the current boundaries of the state-of-the-art. This combination has guaranteed the high quality and optimal industrial exploitation of the project outcomes. This has strengthened the European telecom equipment and semiconductor industry.

The official DRAGON project website is available at the following link: http://www.dragon-project.eu/.