DRAGON

Newsletter
August 2012

Project number: **248277** Project web-site: **www.dragon-project.eu** Project start: **February 2010** Project duration: **02/2010 – 01/2013**

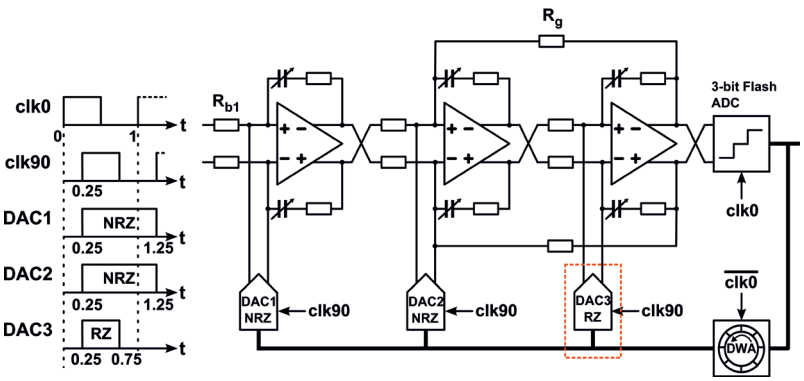


PHOTO: Ericsson AB

Figure 1: CT ΔΣ modulator

Blocking tolerant ΔΣ ADC

As part of a frequency selective ADC a ΔΣ modulator robust to blocking has been designed. Although the modulator is designed for enhanced linearity it has a FOM of 181 fJ / conversion for LTE 20MHz signals. The modulator is implemented in a standard 65nm CMOS technology.

In work package "Innovative Miniaturised Receiver Design" we are set out to design an ADC that is not only comparable to the state-of-the-art with respect to conversion efficiency but also very robust to blocking signals. The goal is to relax the combined complexity and power consumption of an LTE receiver's channel-select filter and ADC.

This design focuses on an ADC that is optimized for a 9 MHz signal bandwidth at baseband suitable for an LTE 20 MHz channel. The low-pass nature of the signal transfer function provided by a feedback continuous-time ΔΣ modulator (Figure 1) is particularly attractive in cellular receivers, as there is no peaking at the pass-band edge where strong interferers may be present.

A relatively low oversampling ratio of 16 is chosen, resulting in a quadrature clock frequency of 288 MHz. The loop filter in the modulator is built with active-RC integrators for high linearity. The amplifiers in the integrators make use of a standard folded-cascode topology (although more power efficient solutions exist [1]). The quantizer is a 3-bit flash ADC with a differential input range of ± 480 mV. A resistive multi-bit feedback DAC [1] (Figure 2) was chosen, as it produces lower thermal noise than the current-steering DAC. The design also includes data-weighted averaging with a 3-bit binary input to randomize static nonlinearities and mismatches.

The modulator is implemented in the ST-Microelectronics 65 nm CMOS technology and occupies an active chip area of 400 µm x 200 µm (Figure 3).

Data-weighted averaging proves to be very effective, reducing the 2nd- and 3rd-order harmonic distortion by 13 dB and 8 dB, respectively, and the noise floor by 2.5 dB. The peak SNR and SNDR are 71 dB and 69 dB, respectively, and occurs at 2.0 dBFS input amplitude.

The design is robust against unfiltered blocking signals. A blocker was applied at 60 MHz offset while the wanted signal, a 20 MHz LTE signal, was at 8 dBFS. Less than 3 dB SNR degradation was measured for a blocking carrier up to 1 dBFS and a 20 MHz LTE signal up to 4 dBFS, respectively. Aliasing of a 282 MHz tone was also measured to be 87 dB.

The total power consumption, including clock buffers, DAC reference voltages, frequency dividers and bias-current generators, is 7.5 mW from a 1.2 V power supply. A figure-of-merit of 181 fJ / conversion is achieved. This result is comparable to other modulators having similar supply voltage, signal bandwidth and SNDR performance, also when subject to blocking signals.

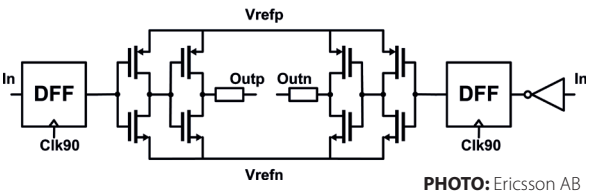


PHOTO: Ericsson AB

Figure 2: Unit NRZ DAC cell

PHOTO: Technikon

Sonia Pichler, editor

Editorial

Dear reader,

the previous issue of this newsletter covered already two interesting project activities: the design of a transceiver chain using Matlab as well as the concept of multi-level-burst mode transmitters. The current edition of our newsletter introduces to you now the design of a ΔΣ modulator robust to blocking signals and describes how the DRAGON project addresses the ambitious goal of optimizing the efficiency of transmitters and power amplifiers in mobile phones.
In addition, the upcoming events are listed for you to have a view on the future conferences where some of the DRAGON results will be presented.
I hope the content of this issue is of interest to you. Any feedback is warmly welcome.

About DRAGON

DRAGON – Design Methods for Radio Architectures GOing Nanoscale- is a specific targeted research project, co-financed by the European Commission under the EU Seventh Framework Programme. The project is running for 36 months from February 2010 to January 2013.

DRAGON aims at developing a design platform comprising multi-standard transceiver specifications and novel flexible architectures in order to break the barriers imposed by the lack of scaling properties of analog components. The interdisciplinary project consortium consists of 7 European partners from industry and academia.

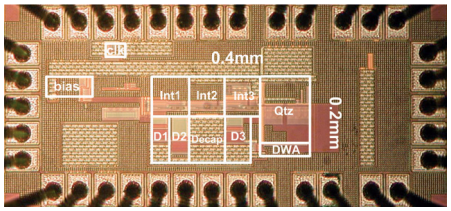


PHOTO: Ericsson AB

Figure 3: Die photograph

[1] P. Shettigar and S. Pavan, "A 15mW 3.6GS/s CT-ΔΣ ADC with 36MHz Bandwidth and 83dB DR in 90nm CMOS," in ISSCC Dig. Tech. Papers, Feb.19—23 2012, pp. 156—157.

[2] S. Pavan et al., "A Power Optimized Continuous-Time ΔΣ ADC for Audio Applications," IEEE J. Solid-State Circuits, vol. 43, no. 2, pp. 351—360, Feb. 2008.

Article Source: Sven Mattisson, Ericsson AB and Mattias Andersson, Lunds Universitet

UPCOMING EVENTS

ESSCIRC - 38th Solid-State Circuits Conference
September 17-21, 2012
Bordeaux, France
www.esscirc2012.org

EuMW 2012 - European Microwave Week
October 28 – November 2, 2012
Amsterdam, The Netherlands
www.eumweek.com

Energy Efficient Transmitters for LTE applications!

It is fortunate that in the quest for either long mobile battery life, or for "green" performance of radio transmitters, the solution is the same: the energy efficiency of the transmit power amplifier must improve. In order to make a major progress in the achievable transmitter's efficiency, meaning a reduction of dissipated power, the major objective of the work package "Smart transmitters and power amplifiers" of the DRAGON project is the efficiency optimization of transmitters and power amplifiers in mobile phones.

PHOTO: KUL

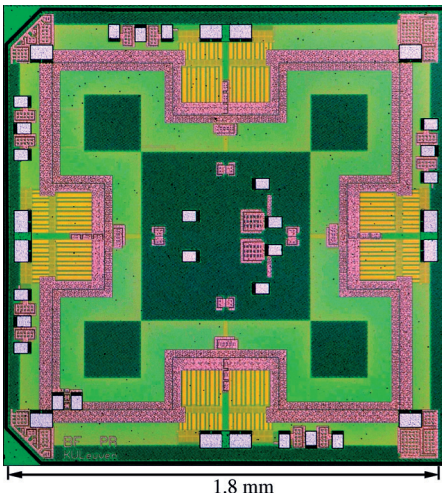


Figure 4: Die photograph of a fully-integrated Watt-level RF PA using a 4-way DAT-combiner for LTE-applications

Standard CMOS is the desired technology for the implementation of low-cost high-volume products. However, the use of a CMOS technology for a PA design introduces some challenges. The power amplifiers designed for this project focus mainly on the two major challenges towards the ultimate LTE RF power amplifier: reaching the watt-level output power in a standard CMOS technology and achieving the power added efficiency at power back-off operation. For this reason, two PAs have been designed during the early months of the project and were taped out in a 90nm standard CMOS technology. On one hand, it will be shown how the one PA reaches the watt-level output power and on the other hand, the Doherty amplifier design accomplishes today's state-of-the art back-off efficiency performance.

In latest research, most of the already reported CMOS PAs do not have sufficient output power nor linearity to cope with the long term evolution (LTE) requirements. In this PA design targeting watt-level output power, a Distributed Active Transformer (DAT) is used to implement a fully-integrated RF power amplifier (PA) for the extended GSM-band and LTE band VIII in a standard 90 nm CMOS process [1]. The DAT allows the designer to integrate both the input and output matching networks as the power combining on the same silicon die. Measurements show that the PA delivers up to ±1 Watt of RF power with 28.4% drain efficiency and 25.8% PAE with only a 2 V supply while achieving a high gain of 28 dB. The choice of optimal biasing ensures a very flat gain and small AM-PM distortion up to high output power. While applying an uplink LTE signal with a PAPR of 6.92 dB, the PA produces 25 dBm of average output power with 15% PAE while obeying the stringent EVM-specifications.

The second PA design is a fully integrated Doherty power amplifier also realized in 90 nm standard CMOS technology [2]. An asymmetrical series combining transformer is used as Doherty combiner to enhance the efficiency at power back-off. The two-stage uneven Doherty The PA has 18 dB gain and delivers 26.3 dBm output power, with a PAE of 33% using 2 V supply. The PAE at 6 dB back-off is still as high as 25.1%. The PA is tested with a 64-QAM modulated signal (PAPR = 10 dB) and a 20 MHz band width. The PA meets the stringent EVM and spectral mask requirements at 19.3 dBm average output power with a PAE of 22.9% with no need of predistortion [2].

PHOTO: KUL

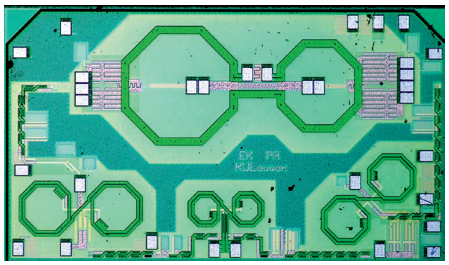


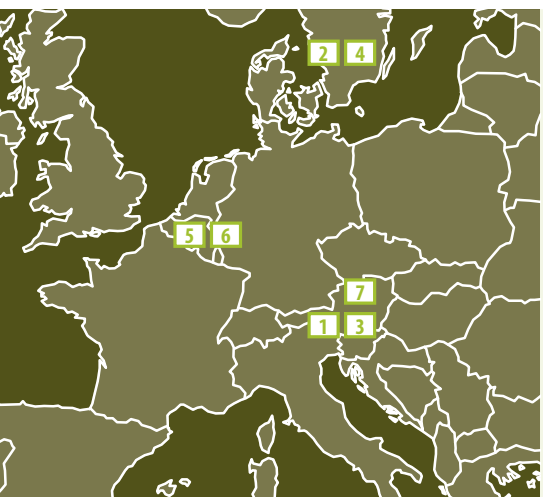
Figure 5: Die photograph of a Transformer-based Uneven Doherty PA for WLAN

These results clearly prove the high efficiency at power back-off and the feasibility of achieving Watt-level output power in standard CMOS while not sacrificing the linearity.

[1] Francois B., Reynaert P.; "A Fully Integrated Watt-Level Linear 900-MHz CMOS RF Power Amplifier for LTE-Applications," Microwave Theory and Techniques, IEEE Transactions on, vol. 60, no. 6, pp. 1878-1885, June 2012.

[2] Kaymaksut E., Reynaert P., "Transformer-Based Uneven Doherty Power Amplifier in 90 nm CMOS for WLAN Applications", Solid-State Circuits, IEEE Journal of, July 2012, Accepted for publication.

Article source: Brecht Francois, Katholieke Universiteit Leuven



Consortium:

1. **Technikon Forschungs- und Planungsgesellschaft mbH (Austria)**
2. **Ericsson AB (Sweden)**
3. **Infineon Technologies Austria AG (Austria)**
4. **Lund University (Sweden)**
5. **Katholieke Universiteit Leuven (Belgium)**
6. **imec (Belgium)**
7. **Graz University of Technology (Austria)**

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SEVENTH FRAMEWORK PROGRAMME

TECHNIKON