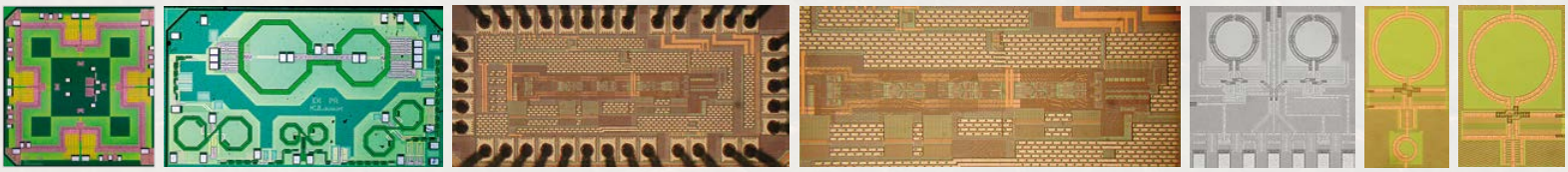
Project number: **248277**
Project website: **www.dragon-project.eu**
Project start: **1st February 2010**
Project end: **31st May 2013**
Project duration: **40 months**
Total Cost: **€ 5.088.435.-**
EC Contribution: **€ 3.480.000.-**

DRAGON

Design Methods for Radio Architectures GOing Nanoscale



Mission of DRAGON

The main objective of the DRAGON project was to research and use new design methodologies and architectural innovations based on reconfigurability and state-of-the-art digital CMOS technology to break the barriers imposed by the lack of scaling properties of analog components. With this concept, distinct reductions in cost, size and energy consumption for multi-standard cellular handsets would be achieved, while higher demands on data rate could be met.

Data rates have been increasing steadily, therefore the energy consumption per transmitted or received data bit needs to be reduced in order to save energy and avoid thermal problems. Wireless data services are becoming an attractive low-cost alternative to be used in novel applications.

The DRAGON Project

In the DRAGON project a design platform comprising an LTE release 10 multi-standard transceiver specification and novel flexible architectures was developed. A number of required external components, such as analog filters, was replaced by reconfigurable digital CMOS (Complementary Metal Oxide Semiconductor) circuitry; and critical building-blocs were implemented to demonstrate proof-of-concept, both of the architecture and design methodology. All critical building-blocks were fabricated, tested, and demonstrated in state-of-the-art CMOS technology. The project results were also provided to standardisation bodies, thus allowing an alignment of requirements to technology limits.

Consortium

The DRAGON consortium has brought together partners and competencies from Europe's leading companies in the areas of nano electronics and wireless communications, one research institute and three universities, with radio chip designers and system experts.

The consortium has covered the full design chain from customer requirements over system integration to hardware design. Top universities were included to achieve optimal innovation and move the current boundaries of the state-of-the-art. This combination has guaranteed the high quality and optimal industrial exploitation of the project outcomes. This has strengthened the European telecom equipment and semiconductor industry.

Project Partners

1 Technikon Forschungs- und Planungsgesellschaft mbH (Austria)

2 Ericsson AB (Sweden)

3 Infineon Technologies Austria AG (Austria)

4 Lund University (Sweden)

5 Katholieke Universiteit Leuven (Belgium)

6 imec (Belgium)

7 Graz University of Technology (Austria)

DRAGON Final Results

The results of DRAGON were achieved in multiple steps and marked by three major milestones, which constituted central points in the course of the project and spanned across the technical work packages.

Milestone 1 – Architectural Exploration

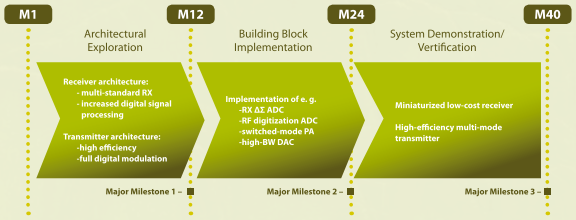
Architectural innovative ideas were identified, explored and used as a high level tool to realise project targets. The focus of the corresponding design experiments was defined.

Milestone 2 – CMOS Building Block Design and Implementation

The most critical building blocks for the targeted multi-standard radio systems with novel architectures were implemented and measured, using state-of-the-art digital CMOS technology.

Milestone 3 – System Demonstration

Silicon system demonstrators were realised and measured. The overall project results were consolidated and verified against the initial goals.



Miniaturized low-cost receiver

- significant area and power reduction by cleverly exploiting digital CMOS process technology speed;
- density advances for implementation of blocks with analog and RF functionality;
- 40% reduction in power consumption;
- 20% reduction in chip area compared to a corresponding conventional solution;
- in the baseband ADC, resolution increased by 9dB at negligible area cost by estimating residue voltage using digital comparators.

High efficiency multi-mode transmitter

- significant improvement in power-added efficiency for integrated CMOS-based transmitter;
- almost 26dBm of peak output power while also capable of delivering 22.5dBm LTE-compliant average output power at 18.9% PAE;
- over 2.5 times better than a similar class-B PA.

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